4.2 A 3W 55% PAE CMOS PA with Closed-Loop 20:1 VSWR Protection

Francesco Carrara[1], Calogero D. Presti[1], Antonino Scuderi[2], Carmelo Santagati[2], Giuseppe Palmisano[1]

[1]Università di Catania, Catania, Italy
[2]STMicroelectronics, Catania, Italy

The design of an efficient PA in a sub-micrometer CMOS technology [1-4] presents a tight trade-off between ruggedness and RF performance, especially at the high power levels required for the low-frequency cellular applications. In saturated applications, CMOS PAs are conveniently operated in a class-E-like mode, with a voltage swing at the output node exceeding 2 to 3 times the supply voltage. Under such a severe voltage stress, Fowler-Nordheim tunnel current through the gate oxide degrades the insulator and device performance, even if no hard oxide breakdown occurs.

Under nominal load conditions, the gate oxide stress can be effectively mitigated by using a combination of thick-oxide transistors and/or cascode topologies [4]. However, device robustness has to be also guaranteed under severely mismatched conditions, which substantially reduce the time to failure due to the increased drain swing occurring at selected load phases. Hence, some kind of VSWR protection is necessary, unless a very conservative and inefficient design is adopted.

In this paper, a CMOS PA is presented, that features both state-of-the-art RF performance and tolerance to severe load VSWR by using a fast and accurate closed-loop protection circuit.

Closed-loop drain overvoltage control [5] can prevent device failure without affecting the RF performance under nominal condition. It has been effectively adopted for the protection of silicon bipolar PAs [6]. This approach is usually implemented according to the block diagram in Fig. 4.2.1(a). The peak voltage at the drain node is detected and then compared to a reference voltage. The feedback loop clamps it to a given safe level by varying the RF gain.

The proposed methodology for detection and comparison in voltage peak control loops is schematically shown in Fig. 4.2.1(b). In the proposed current-mode solution, the comparison function is carried out *before* rectification. Indeed, the output voltage and the reference voltage are both converted into currents and fed to the same circuit node, where comparison is actually performed. Then, the difference current drains to a current rectifier, whose high-impedance output is connected both to an integrating capacitor and to the gain control terminal of the RF chain. It can be shown [7] that the approach in Fig. 4.2.1(b) is functionally equivalent to the one in Fig. 4.2.1(a).

The proposed methodology is able to improve the loop bandwidth, and hence the protection lock-in lag, due to a lower number of poles in the loop frequency response. Indeed, only one low-frequency pole (i.e., the one at C_{PK}) impacts the loop of Fig. 4.2.1(b), whereas two low-frequency poles (i.e., the ones related to the peak detector and comparator) usually affect the loop in Fig. 4.2.1(a). Moreover, the proposed approach features better peak detection accuracy, since it is not affected by the error due to the voltage drop across the rectifying device in classic envelope detectors.

The schematic of the PA is shown in Fig. 4.4.2(a). The RF direct path is a two-stage fully differential amplifier, with on-chip interstage matching. The final stage comprises two 40mm/0.25μm devices (M_3, M_4). The variable-gain first stage is composed of two cross-coupled pseudo-differential pairs (M_1, M_2 and M_{1X}, M_{2X}). When V_{CTRL} is low, transistors M_{1X} and M_{2X} are off and the gain is maximum. As V_{CTRL} is increased, M_{1X} and M_{2X} are turned on by M_{SW} and decrease the net gain of the cell, since the two transconductances cancel each other at the output. It is worth noticing that M_{1X} and M_{2X} produce a beneficial effect on the amplifier stability, since they increase the reverse isolation of the RF chain by compensating the gate-drain capacitance of M_1 and M_2.

Figure 4.2.2(b) shows a detailed schematic of the feedback circuit for peak detection and comparison, which is a double half-wave implementation of Fig. 4.2.1(b). For the purpose of brevity, only one of the two rectifying paths will be described. In transconductor M_5-M_8, resistors R_1 and R_2 along with current mirror M_5-M_6 are exploited to produce difference current $(v_{DG3}–V_{REF}\cdot R_1/R_2)/R_1$ and feed it to the source of M_8, which is the current comparison node. If the peak of v_{GD3} is lower than $V_{REF}\cdot R_1/R_2$, M_8 is off and C_{PK} is precharged to V_{DD} by I_{DIS}. As soon as v_{GD3} peak goes beyond $V_{REF}\cdot R_1/R_2$, current pulses start flowing through M_8 (acting as a current rectifier) and are integrated by C_{PK}. As a consequence, V_{CTRL} is increased and the RF gain is lowered. The loop is compensated by a Miller capacitor across common-source stage M_{13} that pushes the pole at V_{CTRL} node towards higher frequencies, thus improving the loop phase margin. The proposed circuit can also operate with input voltages exceeding the supply range, due to the resistive input. Finally, the topological simplicity results in low area occupation.

The chip is fabricated using 0.25μm CMOS transistors in a BiCMOS process, which offers five metal layers (4μm-thick copper option for the top one) and 5fF/μm² MIM capacitors. Figure 4.2.3 is a micrograph of the PA. The chip size is 1.8×1.8mm² including pads. The circuit is packaged and mounted on a FR4 differential PCB with discrete input and output matching. Measurements are referred to the board connectors. A reference PA without protection is also integrated and characterized for performance comparison.

The output power and PAE versus input power at 870MHz are shown in Fig. 4.2.4. Under a nominal 2V supply, a 3W output power level is achieved with a 55% PAE. The protected and unprotected PA have very similar RF performance, which demonstrates that the loading effect of the protection circuit is negligible. According to measurements, the PA can deliver a saturated output power of as high as 4W when operating at 2.5V. However, higher power levels are traded for efficiency as V_{DD} is increased, due to the lock-in of the protection circuit above the nominal supply voltage.

Load VSWR tests are carried out on a large number of samples. PAs without protection cannot sustain a 10:1 load VSWR when operating at 2V. In contrast, protected PAs revealed no failure after a VSWR test as severe as 20:1 (any phase angle, 0.5dB loss at the output hybrid) under the same supply voltage. These results confirm the effectiveness of the proposed approach.

The dynamics of device degradation are also investigated. The results of the on-wafer reliability test are shown in Fig. 4.2.5. By a multi-harmonic load-pull bench, a 1.3mm unprotected device is operated under optimum load conditions with full-power continuous-wave input at a 2.2V supply (accelerated ageing). Threshold voltage is monitored as a measure of the device degradation versus stress time. A 500mV limit is assumed, since RF performance under saturated operation is relatively insensitive to the threshold voltage shift. Under such conditions, the extrapolated time to failure is about 1000 hours, which means that a nominal 2V supply guarantees a reasonable lifetime for the device.

Acknowledgments:
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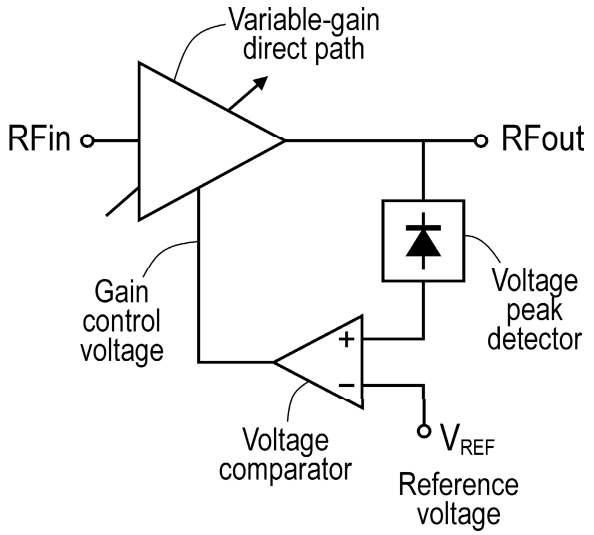

Figure 4.2.1a: VSWR protection through closed-loop drain voltage peak control. Voltage sensing and comparison.

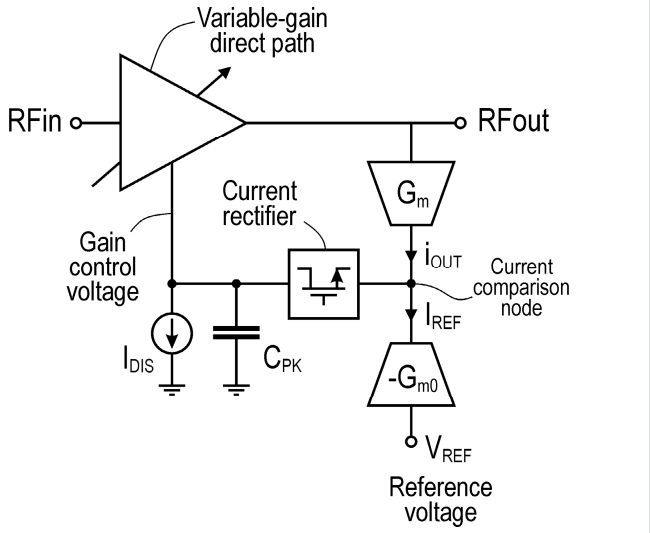

Figure 4.2.1b: VSWR protection through closed-loop drain voltage peak control. Proposed current-mode approach.

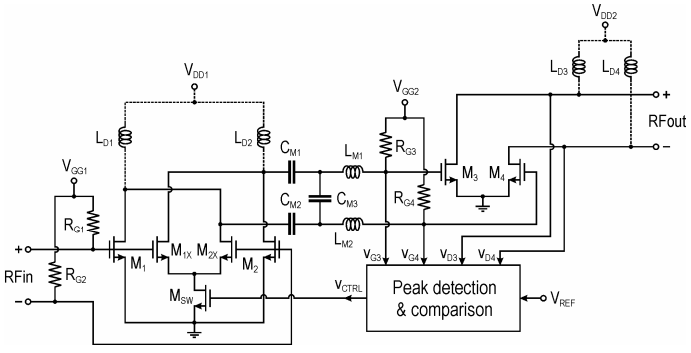

Figure 4.2.2a: Schematic of the power amplifier. Variable-gain RF direct path.

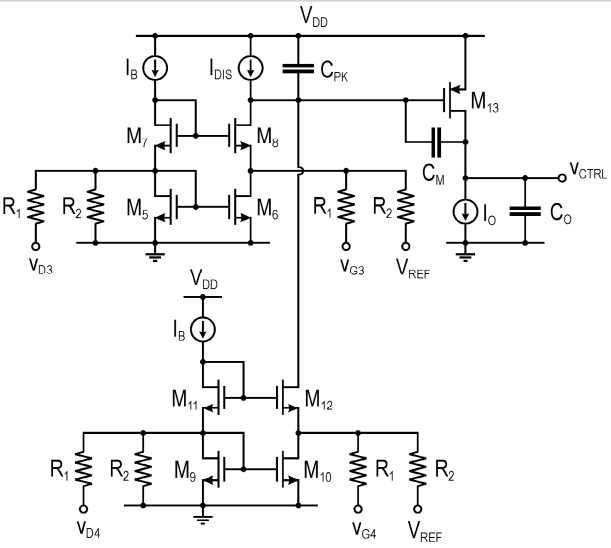

Figure 4.2.2b: Schematic of the power amplifier. Feedback circuit for peak detection and comparison.

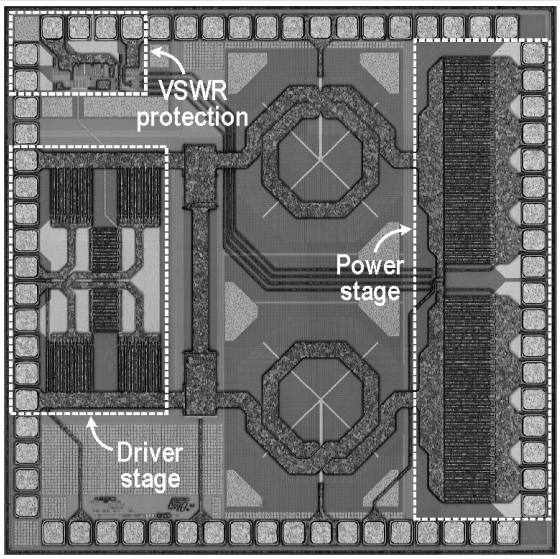

Figure 4.2.3: Die micrograph.

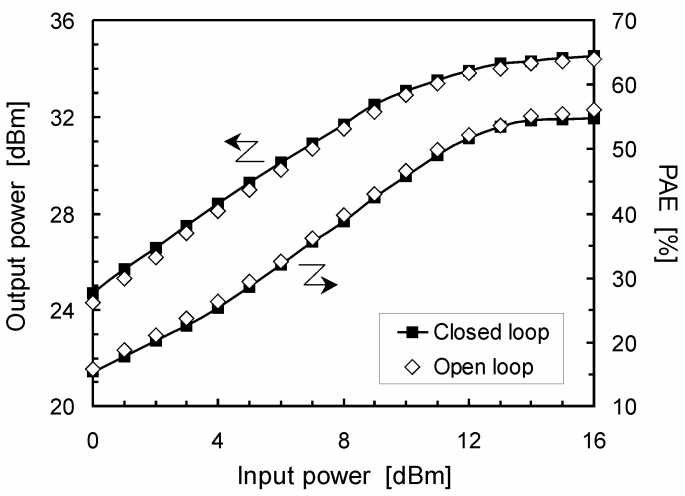

Figure 4.2.4: Measured output power and PAE versus input power (f=870MHz, V_{DD}=2V, T_a=25˚C, pulsed mode test with 1/8 duty cycle).

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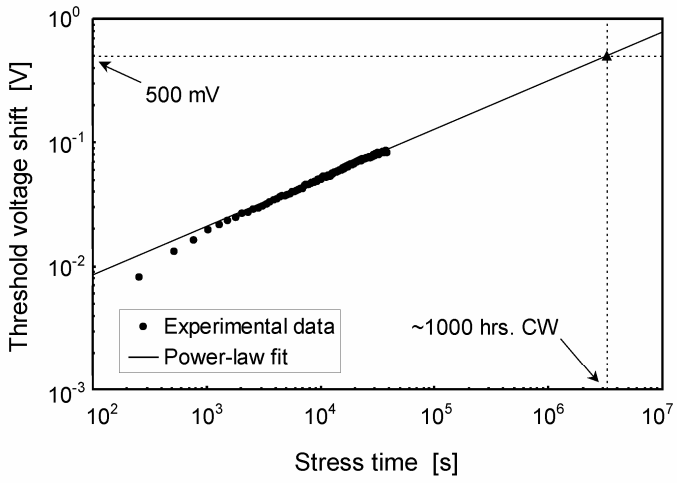

Figure 4.2.5: On-wafer reliability test (accelerated ageing).

